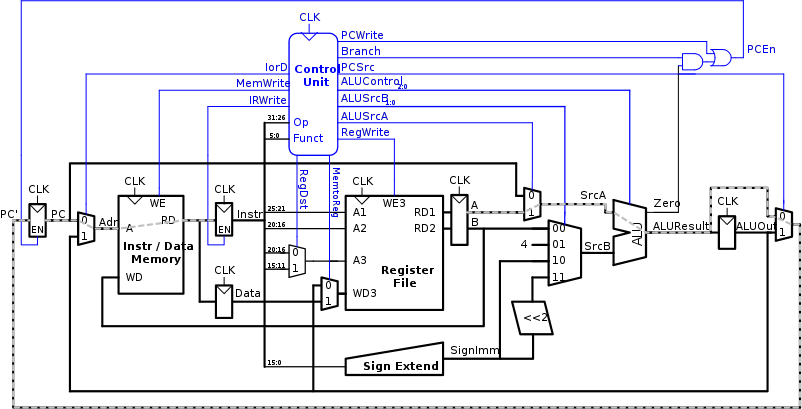
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| Multicycle Processor |
| 412 Final Project |
|  |
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| **5/4/2011** |



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# Multicycle Implementation

The multicycle implementation fixes many of the shortcomings of the single cycle design. The single cycle processor must have a clock period long enough to support the slowest instruction. However the multicycle is not hampered by this limitation. With multicycle, multiple clock cycles with shorter periods are used. Economy of hardware is another weakness of single cycle implementations. Multicycle implementations reuses components of the datapath, making it more cost efficient than the single cycle processor.

Multiple clock cycles allows the processor to break up an instruction into multiple shorter steps. With multicycle, a subset of actions required for one instruction is performed in one cycle. This allows shorter instructions to be executed faster. This process is analogous to a dental office allotting time to patients in multiples of 15 minutes, depending on the amount of work that is anticipated[[1]](#footnote-1). Figure 1 illustrates the single cycle and multicycle clock periods and how clock period affects instruction execution.

Clock

Clock

Instr 2

Instr 1

Instr 3

Instr 4

3 cycles

3 cycles

4 cycles

5 cycles

Time

saved

Instr 1

Instr 4

Instr 3

Instr 2

Time

needed

Time

needed

Time

allotted

Time

allotted

Figure : Multicycle vs Single Cycle

The economy of hardware is addresses by reusing components or combining them. The single cycle uses three adders (two for PC logic and one ALU) and separate memory for data and instructions. The multicycle implementation combines the data and instruction memory and uses one ALU to execute all addition instructions. Adders are expensive circuits because they take up space and require extra transistors.

The design of the multicycle processor is similar to the single cycle. The multicycle processor consists of the datapath and controller block. A controller is added to produce different signals on different steps during execution. These two portions are connected to an external memory. Inside the datapath, combinational logic connects architectural state elements. Non architectural state elements such as registers are used to hold intermediate results between stages.

# Multicycle Datapath

The multicycle datapath builds upon the single cycle. The multicycle datapath has a PC register and a Register File similar to the single cycle datapath. Unlike the single cycle, the multicycle combines the data and instruction memories. Other components such as multiplexers, sign extenders, and ALU are included in the datapath. The full datapath is shown in the figure below.

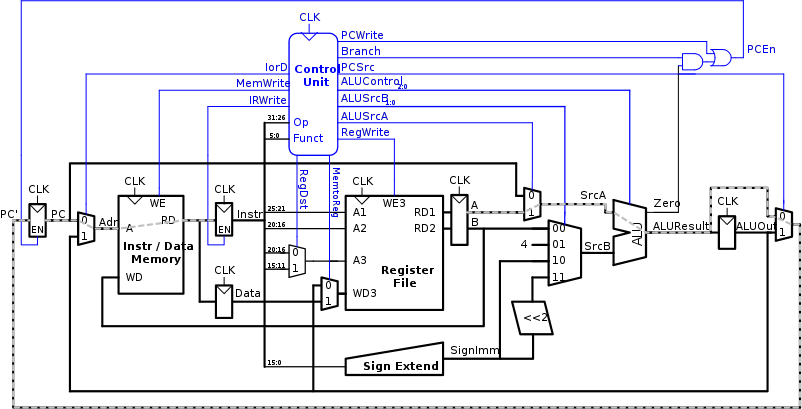


Figure : Multicycle Datapath

The multicycle datapath follows the five stage execution process: Fetch, decode, ALU, data access, and register write. Below are the control signals for the fetch and decode steps.

|  |
| --- |
| IodD = 0 |
| AluSrcA = 0 |
| ALUSrcB = 01 |
| ALUOp = 00 |
| PCSrc = 0 |
| IRWrite = 1 |
| PCWrite = 1 |

Figure 3: Fetch Control Signals

|  |
| --- |
| ALUSrcA = 0 |
| ALUSrcB = 11 |
| ALUOp = 00 |

Figure 4: Decode Control Signals

The fetch control signals are used to calculate PC+4 for the next instruction. The decode control signals are mainly used for branching. After the fetch and decode portions, the datapath of I-type, J-type, and R-type instructions vary.

The load word (lw) and store word (sw) instructions are examples of I-type instructions. After the instruction is decoded, the address for memory access must be computed. This is done by selecting the appropriate control signals. The address for memory access is computed by adding a base address located in the $rs register and a sign extended immediate, ALUSrcA is set to 1, ALUSrcB to 10 and ALUOp to 00. The next step is to use the calculated address to access memory, the control signal IorD is set to 1. For sw, MemWrite is set to 1. The data located in the WriteData (WD) portion is stored to memory. Register $rt is always fed to WD, however the data from $rt is not written to memory unless MemWrite is asserted. Lw has one extra step, to write back to the register. Three control signals are set: RegDst to 0, MemtoReg to 1, and RegWrite to 1. Similar to the memory portion, if RegWrite is not set to 1, the data inside WD3 will not be written to the register file.

If the opcode is an R type instruction, the result must be calculated using the ALU and stored back to the register. To carry out ALU calculation, ALUSrcA is set to 1, ALUSrcB is set to 0, and ALUOp is set to 10. ALUSrcA selects the $rs register to be used as SrcA and ALUSrcB selects $rt register to be used as SrcB of the ALU. ALUOp set to 10 indicates to the controller that ALU operation mode is dependent on the function field of the instruction. For result storage, RegDst and RegWrite are set to 1 and MemtoReg is set to 0. RegDst selects $rd register as the write destination and MemtoReg indicates the data to be written is from ALU. RegWrite serves as a write enable for the Register File.

Whenever a j type instruction is indicated by the opcode, the 26 least significant bits are taken from the instruction and modified as a pseudo direct address. After the instruction is decoded, the PCSrc control signal is set to 10 and the PCWrite to 1. The PCSrc signal allows the ALUResult to circumvent the register and go directly to the PC. The PCWrite makes the or gate of PCEn to produced a 1 and enable the PC register to be overwritten.

To further understand how these datapaths are linked together, a state diagram of the Finite State Machine (FSM) is used. The state diagram is also helpful in gauging the performance of the multicycle processor. The FSM is shown below.

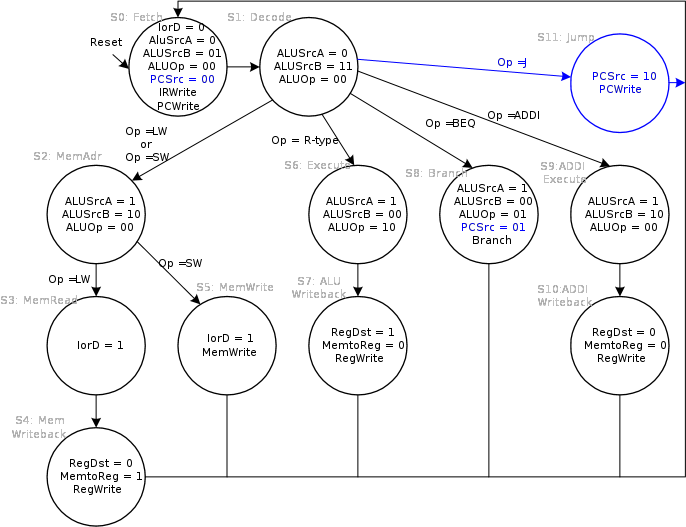


Figure : FSM of Multicycle

# Performance Analysis

The number of cycles and cycle time determine the instruction execution time. Even though the single cycle only used one cycle, the multicycle does less work in a single cycle. The number of cycles per multicycle instruction is equal to the number of stages per instruction. Below is the number of cycles needed for each instruction.

|  |
| --- |
| Load Word = 5 Cycles |
| Store Word = 4 Cycles |
| R –Type = 4 Cycles |
| Branch = 3 Cycles |
| Jump = 3 Cycles |

Figure 5: Required Cycles for Instructions

The cycles per instruction (CPI) of the multicycle processor can be calculated by taking weighted averages of the types of instructions. For example, the SPECINT2000 consists of 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R-type instructions.

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Figure6: CPI Calculation

The CPI of the multicycle is better than the worst case CPI of 5. The single cycle performance is hindered by the worst instruction. The CPI can be used to determine the MIPS of a processor and the execution time. The MIPS of a processor is calculated by dividing the frequency of the processor by its CPI. Execution time is calculated by the following equation

# Verilog Code

# Bibliography

Harris, David Money. Harris, Sarah L. Digital Design and Computer Architecture, San Francisco: Morgan Kaufman Publishers, 2007

Parhami, Behrooz. Computer Architecture, New York: Oxford University Press, 2005

# Reference of Images

Figure 1: Parhami, Behrooz. Computer Architecture

Figure 2: Harris, David Money. Harris, Sarah L. Digital Design and Computer Architecture

Figure 5: Harris, David Money. Harris, Sarah L. Digital Design and Computer Architecture

1. Computer Architecture – Behrooz Parhami [↑](#footnote-ref-1)